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California, Los Angeles. Computer Science Dept) By
Yuval Tamir**

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High Performance multi-queue buffers for VLSI communication switches (1988)

Dynamically-allocated multi- queue buffers for

Communication, Networking Dynamically-allocated multi-queue buffers for VLSI communication switches Full Text Sign-In or Purchase. Sign In

Richard diaz | papers - academia.edu

Richard Diaz studies for the dynamically allocated multi-queue The proposed implementation provides a high-performance solution to buffered communication

Buffer insertion

Buffer insertion is an important technique used to achieve timing closure in high performance VLSI designs. As the number of buffers in ASIC designs has increased

Patent us6766381 - vlsi network processor and

A network processor useful in network switch apparatus and methods of operating such a processor in which data flow handling and flexibility is enhanced by the

Improving direct-mapped cache performance by the

Improving direct-mapped cache performance by the addition of

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Vlsi | priya srinivasan - academia.edu

2013 M.E. VLSI DESIGN I TO IV DSP architectural features/alternatives for high performance and leakage performance trade off multi VT

Patent us8180897 - apparatus and method for

An apparatus in one embodiment handles service requests over a network, wherein the network utilizes a protocol. In this aspect, the apparatus includes: a network

High- performance multiqueue buffers for vlsi

High-performance multiqueue buffers for VLSI communication switches - Co mputer Architecture, 1988. Conference Proceedings. 15th Annual Internati onal Symposium on

Richard diaz - academia.edu

Richard Diaz studies for the dynamically allocated multi-queue The proposed implementation provides a high-performance solution to buffered communication

High performance multi-queue buffers for vlsi

Abstract. Small $n \times n$ switches are key components of multistage interconnection networks used in multiprocessors as well as in the communication coprocessors used in

Yuval tamir, papers and reports - cs | computer

, Fault-Tolerance for High-Performance Multi-Module VLSI Systems of a Multi-Queue Buffer for VLSI Tamir, Performance Optimizations

Lock-free, thread based log buffer implementation,

Sep 28, 2014 for debugging high performance multi-threaded log buffer implementation, for debugging high performance multi free circular array queue.

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High performance set associative translation

A fast low power four-way set-associative translation lookaside buffer (TLB) run modern multi-tasking for high-performance and low-power VLSI systems and

Design and implementation of high-speed

High Performance multi-queue buffers for VLSI allocated multi-queue (DAMQ) buffer, key to the ability of multicomputers to achieve high performance.

Multiport and dual-port memory | idt

offering the most comprehensive line of high-performance dual-port Multi-port can buffer bus speed Multi-port memories are commonly used as

Ieee 2015 project list vlsi - scribd

IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION only for high performance but also similar performance with half the buffer size of a

A vlsi self-compacting buffer for damq

for the dynamically allocated multi-queue A VLSI Self-Compacting Buffer for DAMQ Communication The proposed implementation provides a high-performance

Vlsi computation lab. (vcl) - uc davis department of

Our goal is to discover and develop novel contributions in high-performance, Multi-core architectures; VLSI DSP on Very Large Scale Integration

The multi- queue replacement algorithm for second

High-Performance Computing Overview The Multi-Queue Replacement Algorithm for Second Level Buffer Caches. The Multi-Queue Replacement Algorithm for Second

1.8v lvds clock buffers by idt: low-power, high-

Multi-Queue 3.3V; Sequential Flow-Control Products; Synchronous FIFOs; Memory Interface Products.
1.8V LVDS Clock Buffers by IDT: Low-power, High-performance

Pipelined memory shared buffer for vlsi switches

Department of Computer Science. high performance distributed computing When very large scale integration (VLSI)

Scalable qos-aware memory controller for high

Aug 01, 2015 IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION Abstract This paper proposes a high-performance the reorder buffer for two output queue

Ieee xplore abstract - a vlsi self-compacting

IEEE membership options for an individual and IEEE Xplore for the dynamically allocated multi-queue
The proposed implementation provides a high-performance

Design and evaluation of the combined input and

Computer Science and Packet switches must be able to achieve high the size of the cross point buffers, a distributed input port queue

Buffer pool extension

added high-performance SAS spindles. Also called buffer cache. The buffer pool is a global resource shared by all databases for their cached data pages.

Patent us8028115 - file system adapter for

A file system adapter card that may be plugged into a host computer system for providing hardware-based file system accesses outside the purview of a host operating

Patent us5541914 - packet-switched self-routing

of packet-switched extended generalized-shuffle self-routing multistage interconnection networks provides a continuous performance-cost tradeoff between, on

Proceedings of the 17th conference on advanced

Pipelined Multi-Queue Management in a VLSI ATM Switch Kestrel is a high-performance The Hierarchical Multi-Bank DRAM: A High-Performance Architecture

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Performance tuning network adapters

Aug 14, 2012 such as receive and send buffers, Following are some performance tuning Set the operating system power management profile to High Performance

Hardware support for high-priority traffic in vlsi

High-performance multi-queue buffers for VLSI communication switches. Proc. 15th Annual International Symposium on Computer Architecture, Honolulu, HI

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